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**TITLE: DIFFERENTIAL SAMPLING CIRCUIT FOR GENERATING A DIFFERENTIAL  
INPUT SIGNAL DC OFFSET**

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# **DIFFERENTIAL SAMPLING CIRCUIT FOR GENERATING A DIFFERENTIAL INPUT SIGNAL DC OFFSET**

## **FIELD OF THE INVENTION**

**[0001]** The present invention relates to analog circuits and more particularly to an improved differential sampling circuit based on a switched-capacitor approach that directly generates the real differential signal DC offset value.

## **BACKGROUND OF THE INVENTION**

**[0002]** With the continuous frequency increase of signals used in modern communication links, unwanted effects such as cross talk, false ringing, parasitic reflection, offsets occur more and more often due to the distributed nature of the media which transports these signals. In the particular case of coupled lines, a major contributor is the differential input DC offset which is the result of different amplitudes and common modes on each of the lines. For instance, according to the SCSI standard for hard-disk applications (SPI4) effective to date, data are transported at 80 MHz (frequency of the system clock). At this speed, the data integrity on the bus is high enough so as to generally not require any offset cancellation technique. On the contrary, according to the next SCSI standard to be implemented in the future (SPI5), data will be transported at 160 MHz. At such a high speed, compensation of the differential input signal DC offset becomes necessary. This differential input signal DC offset is sampled and stored in a capacitor; an analog to digital converter (ADC) then converts this value to binary digits and stores it in a register latch.

**[0003]** FIG. 1 illustrates the definition of the differential input signal DC offset. As shown in FIG. 1, the amplitudes and common modes of a differential signal VP-VN are different between the first half and the second half of the period T of the system clock. The differential input signal DC offset is defined as being equal to the half sum of the differential amplitude  $\Delta V1$  in the first half period and the differential amplitude  $\Delta V2$  in

the second half period. The differential input signal DC offset  $\Delta V_{\text{offset}}$  is given by:  
 $0.5 \cdot [(VP1+VP2)-(VN2+VN1)] = 0.5 \cdot [(VP1-VN1)+(VP2-VN2)] = 0.5 \cdot [\Delta V1+\Delta V2]$ .  
This calculation can be performed by a sampling circuit which samples the differential input signal twice within a clock cycle and has a gain of 1/2.

**[0004]** The conventional differential input signal sampling circuit disclosed in “A ratio-independent algorithmic analog-to-digital conversion technique” (IEEE JSSC, vol 19, pp 828-836, December 1984) by P.W. Li, M.J. Chin, P.R. Gray, and R. Castello is of interest in some respects. It is constructed around a differential operational amplifier (opamp) provided with a switched-capacitor network in order to sample twice the differential input signal in four phases to generate  $2 \cdot \Delta V$ , if the input signal keeps its value at times of sampling, or  $[\Delta V1 + \Delta V2]$  if not. However, it does not aim to calculate the differential input signal DC offset, and its gain is independent of both the opamp DC offset and the capacitor values which is a determining advantage.

**[0005]** FIG. 2 shows the single-ended version (simplified diagram) of this conventional differential input signal sampling circuit 20, which samples twice the input signal  $V_{in}$ , to generate a signal  $V_{out} = V_{in} + V_{in} = 2 \cdot V_{in}$ , if input signal  $V_{in}$  remains unchanged during the sampling operations. The single ended version has been chosen in lieu of the differential one for the sake of simplicity of the description. Circuit 20 is organized around an operational amplifier (opamp) 21 and a switched-capacitor network comprising two capacitors C1, C2 and six switches S1-S6 connected as shown in FIG. 2. The positive input of the opamp 21 is coupled to ground. A first capacitor C1, usually referred to as the holding capacitor, is coupled to its negative input and a first node 22. A first switch S1 is coupled between first node 22 and the input signal  $V_{in}$ . A second switch S2 is coupled to first node 22 and ground. A second capacitor C2 is coupled between a second node 23 and the opamp 21 negative input. A third switch S3 is coupled between this negative input and the output of opamp 21. A fourth switch S4 is coupled to second node 23 and the output. A fifth switch S5 is coupled between second node 23 and ground. Finally, a sixth switch S6 is coupled to first node 22 and the output in a feedback loop. Output signal  $V_{out}$  that is generated by circuit 20 is independent of the opamp 21 DC offset  $V_{off}$  and also independent of the value of capacitors C1 and C2. Operation of circuit 20 will be described by reference to FIGS. 3a-3d. In successive drawings, the

status of switches S1-S6 changes. They can be opened or closed according to the application algorithm.

**[0006]** Full operation of circuit 20 requires four phases: two input signal sampling and two charge transfers. Considering FIG. 3a, let us assume the input signal to be sampled  $V_{in}$  is equal to  $V_1$ . It is easy to calculate voltage  $V_{c1}$  across capacitor  $C_1$ , voltage  $V_{c2}$  across capacitor  $C_2$  and output voltage  $V_{out}$ . At the end of the first input signal sampling, we have:

$$V_{c1} = V_1 - V_{off}$$

$$V_{c2} = -V_{off}$$

$$V_{out} = V_{off}$$

The charge  $Q_1$  stored into capacitor  $C_1$  is equal to  $C_1 \cdot (V_1 - V_{off})$ .

**[0007]** After the first sampling, the first charge transfer is performed using the configuration shown in FIG. 3b. The charge variation  $DQ_1 = C_1 \cdot V_1$  is transferred to capacitor  $C_2$ . We then have:

$$V_{c1} = -V_{off}$$

$$V_{c2} = -V_{off} + V_1 \cdot C_1 / C_2$$

$$V_{out} = V_1 \cdot C_1 / C_2$$

The first sampling and the first charge transfer described above by reference to FIGS. 3a-3b are performed during the first half period of the system clock.

**[0008]** Next, the second input signal sampling is performed using the configuration depicted in FIG. 3c. After the second input sampling, we assume that  $V_{in}$  has changed and is now equal to  $V_2$ . We have:

$$V_{c1} = V_2 - V_{off}$$

$$V_{c2} = -V_{off} + V_1 \cdot C_1 / C_2 \text{ (} V_{c2} \text{ remains unchanged)}$$

$$V_{out} = V_{off}$$

[0009] Finally, the second charge transfer is performed using the configuration shown in FIG. 3d. At the end of this step, the charge Q2 stored on C2 is transferred to capacitor C1 so that we have:

$$V_{c2} = -V_{off}$$

$$DQ2 = V1 * C1$$

$$V_{c1} = V2 - V_{off} + DQ2 / C1 = V2 - V_{off} + V * C1 / C1 = V1 + V2 - V_{off}$$

$$V_{out} = V_{off} + V_{c1} = V1 + V2$$

[0010] The second sampling and the second charge transfer described above by reference to FIGS. 3c-3d are performed during the second half period of the system clock. The operations described above by reference to FIGS. 3a-d are thus performed at each system clock cycle.

[0011] Consequently, using circuit 20, Vout equals the sum of the two sampled input values V1 and V2. It is to be noted that Vout is independent of both the opamp 21 DC offset Voff and the values of capacitors C1 and C2, which is beneficial. However, should we consider the differential version of circuit 20 applied to the calculation of the differential DC offset  $\Delta V_{offset}$ , it would generate a differential voltage equal to  $[\Delta V1 + \Delta V2]$ , so that it would have the inconvenience of requiring a 1/2 gain opamp connected in series at its outputs before obtaining the differential offset value which is equal to  $0.5 * [\Delta V1 + \Delta V2]$ .

## SUMMARY OF THE INVENTION

[0012] According to the present invention there is described an improved differential sampling circuit based on a switched-capacitor network approach that directly generates the real differential input signal DC offset value. It is configured around a differential operational amplifier and is provided with a pair of switched-capacitor networks, each including an innovative block to generate the real value of the differential input signal DC offset at each system clock cycle. During the first half cycle, the differential input signal pair is sampled and the holding capacitors in each network are charged. During the

second half cycle, the differential input signal pair is sampled again and the holding capacitors are further charged. At the end of the cycle, the charges held in the holding capacitors are applied to the differential operational amplifier, so that the differential output signal that is output therefrom is equal to the real differential input signal DC offset value.

**[0013]** It is therefore a primary object of the present invention to provide an improved differential sampling circuit based on a switched-capacitor network approach that directly generates the real differential input signal DC offset value.

**[0014]** It is another object of the present invention to provide an improved differential sampling circuit configured around a differential operational amplifier and a pair of switched-capacitor network wherein the differential input signal DC offset value is independent of the differential operational amplifier DC offset.

**[0015]** It is still another object of the present invention to provide an improved differential sampling circuit based on a switched-capacitor network approach that directly generates the differential input signal DC offset value with a high accuracy to meet the SCSI-PI5 specifications.

**[0016]** In accordance with the present invention, a differential sampling circuit is provided for generating a real differential input signal DC offset value at each period of a system clock. The circuit includes a differential operational amplifier and two capacitors. The operational amplifier has an input terminal and an output terminal, and is characterized by a DC offset voltage; the capacitors each have a first terminal connected to the input terminal, and are matched with respect to capacitance value. During an input signal sampling operation in a portion of each system clock period, the charge on the first capacitor is proportional to the DC offset voltage, and the first capacitor and the second capacitor are connected in parallel during a charge transfer operation in a subsequent portion of each system clock period. The output terminal voltage during the charge transfer operation is proportional to a sum of a first input voltage applied to the input terminal during the first signal sampling operation and a second input voltage applied to the input terminal during a second signal sampling operation in another portion of the system clock period; this output terminal voltage is independent of the DC offset voltage.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0017] FIG. 1 illustrates the general definition of the differential input signal DC offset.

[0018] FIG. 2 is a schematic diagram of a conventional single-ended input signal sampling circuit.

[0019] FIGS. 3a-d shows different configurations of the circuit of FIG. 2, to illustrate four operational phases of that circuit respectively.

[0020] FIG. 4 shows a single-ended input signal sampling circuit in accordance with an embodiment of the present invention.

[0021] FIGS. 5a-d show different configurations of the FIG. 4 circuit to illustrate four operational phases thereof.

[0022] FIG. 6 is a schematic diagram of a differential sampling circuit embodying the present invention and derived from the circuit of FIG. 4, for generating the real differential input signal DC offset value.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0023] Like reference numerals (with prime) are used in the drawings to designate identical (corresponding) parts. For the sake of illustration, the circuit 20 shown in FIG. 2, will be first modified to generate  $0.5*(V1+V2)$  instead of  $(V1+V2)$  according to the present invention.

[0024] As apparent from FIG. 4, where a circuit embodying the invention is referenced 40, the circuit of FIG. 2 has been modified to add circuit block 41. Circuit block 41 comprises one extra capacitor C0 and two extra switches S7 and S8. Capacitor C0 is coupled to the opamp 21 negative input and to a third node 42. Switch S7 is coupled to second node 42 and ground. Switch S8 is connected between the first and third nodes.

**[0025]** The operation of circuit 40 is still based upon four operational phases that will be now described with reference to FIGS 5a-5d; these phases are performed at each system clock cycle.

**[0026]** Let us consider FIG. 5a which illustrates the first input signal sampling. It may still be assumed that  $V_{in} = V_1$ . When  $V_1$  is sampled, the capacitor  $C_0$  is floating as switches  $S_7$  and  $S_8$  are open. Switches  $S_2$ ,  $S_4$  and  $S_6$  are open while switches  $S_1$ ,  $S_3$  and  $S_5$  are closed. After the first input signal sampling, we have:

$$V_{c1} = V_1 - V_{off}$$

$$V_{c2} = -V_{off}$$

$$V_{out} = V_{off}$$

The charge  $Q_1$  stored into holding capacitor  $C_1$  is equal to  $C_1 \cdot (V_1 - V_{off})$ .

**[0027]** FIG. 5b illustrates the configuration of circuit 40 during the first charge transfer when switches  $S_1$ ,  $S_3$  and  $S_5$  are opened and switches  $S_2$  and  $S_4$  are closed. During this phase, the charge variation  $DQ_1$ , equal to  $C_1 \cdot V_1$ , is transferred into capacitor  $C_2$ , so that:

$$V_{c1} = -V_{off}$$

$$V_{c2} = -V_{off} + V_1 \cdot C_1 / C_2$$

$$V_{out} = V_1 \cdot C_1 / C_2$$

**[0028]** During the second input sampling, switches  $S_1$ ,  $S_3$  and  $S_7$  are closed and switches  $S_2$  and  $S_4$  are opened, circuit 40 then has the configuration depicted in FIG. 5c. Let us assume now that  $V_{in}$  has changed and equals  $V_2$ . The capacitor  $C_0$  is connected to ground because switch  $S_7$  is closed, so that:

$$V_{c0} = -V_{off}$$

$$V_{c1} = V_2 - V_{off}$$

$$Q_1 = C_1 \cdot (V_2 - V_{off})$$

$$V_{c2} = -V_{off} + V_1 \cdot C_1 / C_2 \quad (V_{c2} \text{ remains unchanged})$$

$$V_{out} = V_{off}$$

The charge  $Q_0$  stored into capacitor  $C_0$  is equal to  $-C_0 \cdot V_{off}$ . This is an important feature of the present invention as will be discussed in more detail below. The charge stored in capacitor  $C_2$  is equal to  $V_1 \cdot C_1 - C_2 \cdot V_{off}$ .

[0029] Finally, during the second charge transfer (see FIG. 5d), switches  $S_1$ ,  $S_3$  and  $S_7$  are opened while switches  $S_5$ ,  $S_6$  and  $S_8$  are closed. The capacitor  $C_0$  is put in parallel with capacitor  $C_1$  because switch  $S_8$  is closed. Then:

$$V_{c2} = -V_{off}$$

$$Q_2 = -V_{off} \cdot C_2$$

$$V_{c0} = V_{c1} = (Q_0 + Q_1) / (C_0 + C_1) = (C_1 \cdot V_2 - V_{off}(C_0 + C_1)) / (C_0 + C_1) = V_2 \cdot C_1 / (C_0 + C_1) - V_{off}$$

There is a charge transfer equal to the charge variation  $DQ_2$  to capacitors  $C_0$  and  $C_1$ . Consequently, the voltages  $V_{c0}$  and  $V_{c1}$  change as follows:

$$DQ_2 = C_1 \cdot V_1$$

$$V_{c0} = V_{c1} = (DQ_2 + Q_0 + Q_1) / (C_0 + C_1) = C_1 \cdot V_1 / (C_0 + C_1) + V_2 \cdot C_1 / (C_0 + C_1) - V_{off}$$

$$V_{c0} = V_{c1} = (V_1 + V_2) / (1 + C_0/C_1) - V_{off}, \text{ and finally}$$

$$V_{out} = V_{c0} + V_{off} = (V_1 + V_2) / (1 + C_0/C_1).$$

[0030] Because  $Q_0 = -C_0 \cdot V_{off}$  is present in the calculation of  $V_{c0}$ , the opamp 21 DC offset  $V_{off}$  does not appear in  $V_{out}$ . As a result, the signal output from circuit 40 is still independent of the opamp 21 offset, and is independent of the value of capacitor  $C_2$  as well. It is noteworthy that, if  $C_0 = C_1$ , i.e. if there is a perfect matching between these capacitors, then  $V_{out} = 0.5 \cdot (V_1 + V_2)$ ; otherwise, the error on  $V_{out}$  is divided by two. For instance, if the mismatch between  $C_0$  and  $C_1$  is equal to about 2%, the error on  $V_{out}$  will be only about 1%. Only the ratio  $C_0/C_1$  of capacitor values must be as close as possible to 1. An improved differential sampling circuit embodying the present invention and

derived from circuit 40, for generating the real differential input signal DC offset, embodying the present invention, will be now described in detail.

[0031] Circuit 60, shown in FIG. 6, may be viewed as a combination of two identical circuits 40 driven by first and second input signals  $V_{in+}$  and  $V_{in-}$  respectively. However, in the embodiment of the present invention shown in FIG. 6, the two opamps have been merged in a single differential opamp referenced 61, having thus two inputs and two outputs, for greater optimization. As apparent in FIG. 6, the upper switched-capacitor network 62', which includes circuit block 41', is connected between the positive input and the negative output. Likewise, the lower switched-capacitor network 62'', which includes block 41'', is connected between the negative input and the positive output. In the upper network, the extra devices are referenced  $C0'$ ,  $S7'$  and  $S8'$ . In the lower network, the extra devices are referenced  $C0''$ ,  $S7''$  and  $S8''$ . It is highly desirable that the corresponding components in the upper and lower networks be matched. The input signals applied to circuit 60, forming the differential input signal pair, are labeled  $V_{in+}$  and  $V_{in-}$ . Corresponding output signals are labeled  $V_{out-}$  and  $V_{out+}$  respectively, defining a differential output signal  $\Delta V_{out}$  therebetween. By construction, this differential output signal  $\Delta V_{out}$  that is generated by circuit 60 is equal to the differential input signal DC offset  $\Delta V_{offset}$ , as soon as the four operational phases have been completed.  $V_{out-} = 0.5 * [(V_{in+1}) + (V_{in+2})]$ ,  $V_{out+} = 0.5 * [(V_{in-1}) + (V_{in-2})]$  using the calculations and the notations given above for the improved circuit 40 described by reference to FIGS. 4 and 5a-d, so that  $\Delta V_{out} = (V_{out-}) - (V_{out+}) = \Delta V_{offset} = 0.5 * [\Delta V1 + \Delta V2]$ , wherein  $\Delta V1 = [(V_{in+1}) - (V_{in-1})]$  and  $+\Delta V2 = [(V_{in+2}) + (V_{in-2})]$ , i.e. to the half sum of the two sampled differential input signal values.

[0032] Simulations have demonstrated that it is possible to measure the real value of the differential input signal DC offset and then to meet the SCSI-PI5 specifications.

[0033] The advantages of the invention are as follows: The differential input signal DC offset value is measured during only one system clock period. The DC offset is independent of the differential opamp 61 DC offset and the values of capacitors. Only the capacitor value ratio  $C0/C1$  should be equal to 1; a mismatch in this ratio of x% would lead to an error of x/2 % in the measured DC offset value.

**[0034]** While the invention has been particularly described with respect to a preferred embodiment thereof, it should be understood by one skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.

**[0035]** We claim: